Patent claims

1. A method for producing a binary information memory cell,
in which
- a first electrically conductive region is produced in and/or on a substrate;
- a second electrically conductive region is produced at a prescribed distance from the first electrically conductive region such that a cavity is formed between the first and second electrically conductive regions;
- the first and second electrically conductive regions are set up such that upon application
  - of a first voltage to the electrically conductive regions a structure which at least partially bridges the distance between the electrically conductive regions is formed in from material from at least one of the electrically conductive regions;
  - of a second voltage to the electrically conductive regions material from a structure which at least partially bridges the distance between the electrically conductive regions is taken back.

2. The method as claimed in claim 1,
in which the prescribed distance between the first and second electrically conductive regions is formed by producing an auxiliary structure of prescribed thickness on the first electrically conductive region and removing the auxiliary structure after the second electrically conductive region is formed.

3. The method as claimed in claim 2,
in which the auxiliary structure used is a self-assembled monolayer.

4. The method as claimed in claim 2,
in which the auxiliary structure is produced using an atomic layer deposition method.

5. The method as claimed in claim 2,
in which the auxiliary structure is produced using a molecular beam epitaxy method.

6. The method as claimed in one of claims 1 to 5,
in which the prescribed distance is between approximately 0.5 nm and approximately 5 nm.

7. The method as claimed in one of claims 1 to 6,
in which the prescribed distance is between approximately 0.6 nm and approximately 2 nm.

8. The method as claimed in one of claims 1 to 7,
in which the first electrically conductive region is a first interconnect and the second electrically conductive region is a second interconnect, which interconnects are produced so as to run toward one another essentially at right angles.

9. A binary information memory cell

- having a substrate;
- having a first electrically conductive region produced in and/or on the substrate;
- having a second electrically conductive region which is arranged at a prescribable distance from the first electrically conductive region such that a cavity is formed between the first and second electrically conductive regions;
- where the first and second electrically conductive regions are set up such that upon application
    - of a first voltage to the electrically conductive regions a structure which at least partially bridges the distance between the electrically conductive regions is formed in

freely growing fashion from material from at least one of the electrically conductive regions;

- of a second voltage to the electrically conductive regions material from a structure which at least partially bridges the distance between the electrically conductive regions is taken back.

10. The binary information memory cell as claimed in claim 9,
in which the substrate is a silicon substrate.

11. The binary information memory cell as claimed in claim 9 or 10,
in which the first or the second electrically conductive region has

- a solid-state electrolyte,
- a glass comprising metal ions
- a semiconductor comprising metal ions; or
- a chalcogenide.

12. The binary information memory cell as claimed in one of claims 9 to 11,
in which the first or the second electrically conductive region comprises silver sulfide.

13. The binary information memory cell as claimed in one of claims 9 to 12,
in which the first or the second electrically conductive region is made of metallic material.

14. The binary information memory cell as claimed in one of claims 9 to 13,
in which the first or the second electrically conductive region comprises

- silver;
- copper;

- aluminum;
- gold and/or
- platinum.

15. A binary information memory cell arrangement having a plurality of binary information memory cells as claimed in one of claims 9 to 14.

16. The binary information memory cell arrangement as claimed in claim 15,
in which the binary information memory cells are arranged essentially in matrix form.

17. The binary information memory cell arrangement as claimed in claim 15 or 16,
in which selection elements for selecting a binary information memory cell are produced in and/or on the substrate for at least some of the binary information memory cells.

18. The binary information memory cell arrangement as claimed in claim 17,
in which the selection elements are field effect transistors.

19. The binary information memory cell arrangement as claimed in claim 18,
in which the selection elements are vertical field effect transistors.